WHAT IS CLAIMED IS:

1. An encoder, comprising:
a state machine configured to generate a plurality of state bits; and
an interface configured to couple an input relating to one of the state bits into the state machine during a time period.

2. The encoder of claim 1 wherein the interface comprises a switch.

3. The encoder of claim 1 wherein the interface is configured to couple an input signal into the state machine during a second time period, and coupled said one of the state bits into the state machine during the time period.

4. The encoder of claim 1 wherein the interface is configured to couple an input signal into the state machine during a second time period, and couple a complement of said one of the state bits into the state machine during the time period.

5. The encoder of claim 1 further comprising an output including a second one of the state bits.

6. The encoder of claim 5 wherein the interface comprises an output, the encoder output further including the interface output.

7. The encoder of claim 1 wherein the state machine comprises a 2^p-state finite state machine where p comprises an integer greater than one.

8. The encoder of claim 1 wherein the state machine includes at least two delay registers configured to delay the plurality of state bits.

9. The encoder of claim 8 wherein the state machine includes an adder coupled to one of the delay registers.

10. An encoder, comprising:
state generation means for generating a plurality of state bits; and

interface means for coupling an input relating to one of the state bits into the state generation means during a time period.

11. The encoder of claim 10 wherein the interface means comprises a switch.

12. The encoder of claim 10 wherein the interface means is configured to couple an input signal into the state generation means during a second time period, and coupled said one of the state bits into the state machine during the time period.

13. The encoder of claim 10 wherein the interface means is configured to couple an input signal into the state generation means during a second time period, and coupled a complement of said one of the state bits into the state machine during the time period.

14. The encoder of claim 10 further comprising an output including a second one of the state bits.

15. The encoder of claim 14 wherein the interface comprises an output, the encoder output further including the interface output.

16. The encoder of claim 10 wherein the state generation means comprises a 2^p-state finite state machine where p is an integer greater than one.

17. The encoder of claim 10 wherein the state generation means includes at least two delay registers configured to delay the plurality of state bits.

18. The encoder of claim 17 wherein the state generation means includes an adder coupled to one of the delay registers.

19. A transmitter, comprising:

an encoder having,

a state machine configured to generate a plurality of state bits, and

an interface configured to couple an input relating to one of the state bits into the state machine during a time period; and

an RF stage coupled to the encoder.

20. The encoder of claim 19 wherein the interface comprises a switch.

21. The encoder of claim 19 wherein the interface is configured to couple an input signal into the state machine during a second time period, and coupled said one of the state bits into the state machine during the time period.

22. The encoder of claim 19 wherein the interface is configured to couple an input signal into the state machine during a second time period, and coupled a complement of said one of the state bits into the state machine during the time period.

23. The encoder of claim 19 further comprising an output including a second one of the state bits.

24. The encoder of claim 23 wherein the interface comprises an output, the encoder output further including the interface output.

25. The transmitter of claim 19 wherein the state machine comprises a 2^p-state finite state machine where p comprises an integer greater than one.

26. The transmitter of claim 19 wherein the state machine includes at least two delay registers configured to delay the plurality of state bits.

27. The transmitter of claim 26 wherein the state machine includes an adder coupled to one of the delay registers.

28. The transmitter of claim 19 further comprising a transmit control unit coupled to the encoder, the transmit control unit being configured to control the interface.

29. The transmitter of claim 28 further comprising a preamble generator coupled to the transmit control logic unit.

30. The transmitter of claim 28 further comprising a CRC generator coupled to the transmit control logic unit.

31. A transmitter, comprising:

an encoder having,

state generation means for generating a plurality of state bits, and

interface means for coupling an input relating to one of the state bits into the state generation means during a time period; and

an RF stage coupled to the encoder.

32. The transmitter of claim 31 wherein the interface means comprises a switch.

33. The transmitter of claim 31 wherein the interface means is configured to couple an input signal into the state generation means during a second time period, and couple said one of the state bits into the state machine during the time period.

34. The transmitter of claim 31 wherein the interface means is configured to couple an input signal into the state generation means during a second time period, and couple a compliment of said one of the state bits into the state machine during the time period.

35. The transmitter of claim 31 further comprising an output including a second one of the state bits.

36. The transmitter of claim 35 wherein the interface comprises an output, the encoder output further including the interface output.

37. The transmitter of claim 31 wherein the state generation means comprises a 2^p-state finite state machine where p is an integer greater than one.

38. The transmitter of claim 31 wherein the state generation means includes at least two delay registers configured to delay the plurality of state bits.

39. The transmitter of claim 38 wherein the state generation means includes an adder coupled to one of the delay registers.

40. The transmitter of claim 31 further transmit control means for controlling the interface means to couple the input relating to one of the state bits into the state generation means during the time period; and

41. The transmitter of claim 40 further comprising means for generating a preamble coupled to the transmit control means.

42. The transmitter of claim 40 further comprising means for generating a CRC coupled to the transmit control means.

43. An encoder, comprising:

a state machine configured to generate a state; and

an interface configured to serially couple an input relating to a binary representation of the state into the state machine during a time period.

44 The encoder of claim 43 wherein the interface is configured to serially couple a plurality of input signals into the state machine during a second time period, and serially couple the binary representation of the state at the end of the second period into the state machine during the time period.

45 The encoder of claim 43 wherein the interface is configured to serially couple a plurality of input signals into the state machine during a second time period, and serially couple a compliment of the binary representation of the state at the end of the second period into the state machine during the time period.

46. The encoder of claim 43 wherein the interface comprises a switch configured to serially couple the input signals into the state machine during the second time period, and serially couple the input relating to the binary representation of the state at the end of the second period into the state machine during the time period.

47. The encoder of claim 43 wherein the state machine comprises a 2^p-state finite state machine where p comprises an integer greater than one.

48. The encoder of claim 43 wherein the state machine includes at least two delay registers configured to generate the state.

49. The encoder of claim 48 wherein the state machine includes an adder coupled to one of the delay registers.

50. An encoder, comprising:

state generation means for generating a state; and

interface means for serially coupling an input relating to a binary representation of the state into the state machine during a time period.

51. The encoder of claim 50 wherein the interface means is configured to serially couple a plurality of input signals into the state generation means during a second time period, and serially couple the binary representation of the state at the end of the second period into the state generation means during the time period.

52. The encoder of claim 50 wherein the interface comprises a switch configured to serially couple the input signals into the state generation means during the second time period, and serially couple a compliment of the binary representation of the state at the end of the second period into the state generation means during the time period.

53. The encoder of claim 50 wherein the state generation means comprises a 2^p-state finite state machine where p comprises an integer greater than one.

54. The encoder of claim 50 wherein the state generation means includes at least two delay registers configured to generate the state.

55. The encoder of claim 54 wherein the state generation means includes an adder coupled to one of the delay registers.

56. A method of generating a signal, comprising:

generating a payload as a function of a state machine output;

generating a tail as a function a binary representation of the state machine output at the end of the payload generation; and

appending the tail to the payload.

57. The method of claim 56 wherein the state machine output comprises a plurality of state bits, the tail generation comprising serially feeding the state bits for the binary representation of the state machine output at the end of the payload generation into the state machine.

58. The method of claim 56 wherein the state machine output comprises a plurality of state bits, the tail generation comprising serially feeding a compliment for each of the state bits for the binary representation of the state machine output at the end of the payload generation into the state machine.

59. The method of claim 56 wherein the state machine output comprises a plurality of first state bits having a most significant bit, the tail generation comprising feeding the most significant bit of the first state bits into the state machine during a first clock cycle to generate a second plurality of state bits having a most significant bit, and feeding the most significant bit of the second state bits into the state machine during a second clock cycle.

60. The method of claim 59 wherein the first state bits further comprise a least significant bit, and wherein the most significant bit of the second state bits is the least significant bit of the first state bits.

61. The method of claim 56 wherein the state machine output comprises a plurality of first state bits having a most significant bit, the tail generation comprising feeding a compliment of the most significant bit of the first state bits into the state machine during a first clock cycle to generate a second plurality of state bits having a most significant bit, and feeding a compliment of the most significant bit of the second state bits into the state machine during a second clock cycle.

62. The method of claim 61 wherein the first state bits further comprise a least significant bit, and wherein the most significant bit of the second state bits is the least significant bit of the first state bits.